Planar Implantation Edge Termination for Vertical GaN Power Devices

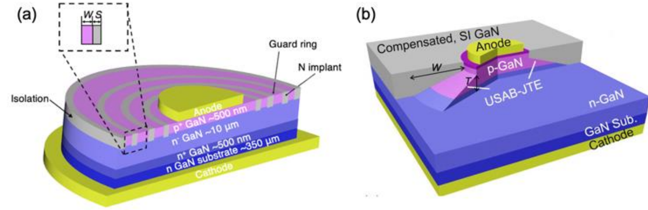

Fig.1 (a) GR (guard ring) 3D structure schematics (b) USAB-JTE (ultra-small-angle bevel-junction termination extension) 3D structure schematics

In high power, high voltage gallium nitride (GaN) vertical devices, edge termination is essential for managing E-field crowding at the edge and achieving the desired breakdown voltage. In this work, the two methods—GR and USAB-JTE—both utilize single-step ion implantation to accomplish isolation and edge termination. The single-implantation technique does not require precise control of implantation depth and obviates the need for GaN etching, enabling a great process latitude and less fabrication complexity.

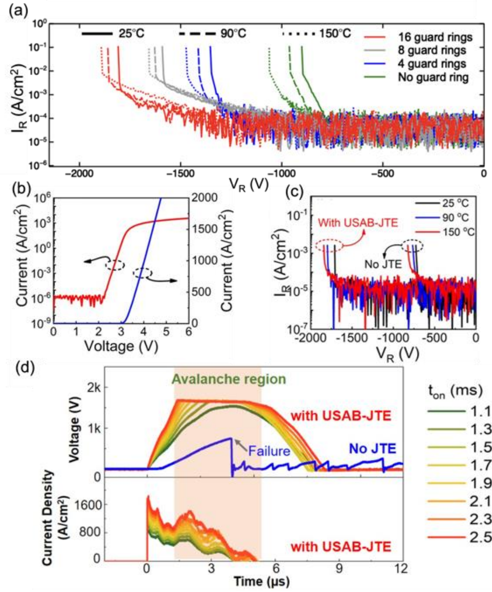

Fig.2 (a) Guard ring devices showing positive temperature coefficient for breakdown voltage (BV) and relationship between ring count, ring spacing *S* and BV (b) Forward bias characteristics for USAB-JTE devices, guard ring devices have similar curve (c) USAB-JTE devices showing positive temperature coefficient for BV (d) USAB-JTE demonstrates avalanche robustness under unclamped inductive switching (UIS) test.

Fig.1 (a) shows the 3D schematics for GR structure. *W* and *S* refer to widths and spacings, where width is the unimplanted p-GaN region and spacing is the implanted isolation region. *W* and *S* vary from 1 μm to 2.5 μm and 1 μm to 2 μm, respectively. The active area is surrounded by implanted rings. Fig. 1 (b) shows the 3D schematic of USAB-JTE. The uncompensated p-GaN at the device edge exhibits a wedge shape with a large ratio between the JTE width *W* and thickness *T*. Both devices are based on wafers provided by Enkris semiconductor Inc.

Fig. 2 (a) shows the reverse I-V characteristics of the GR devices with only the implanted isolation (i.e., no rings) and those with 4, 8, and 16 rings (*S* = 1.1 μm and *W* = 2.4 μm). A clear trend of increased BV over increased spacing is observed. Positive temperature coefficient of breakdown voltage is demonstrated on all devices measured, suggesting a uniform avalanche breakdown capability. Meanwhile, as ring count increases, the BV increases and eventually reaches saturation. Fig. 2 (b) shows forward-bias characteristics for USAB-JTE devices. The IV forward curves for GR devices are similar to those of USAB-JTE because they are based on the same wafer. An on-off ratio of 10^9 and a current density of ~1700A/cm^2 are achieved. Fig. 2 (c) demonstrates the positive temperature coefficients of USAB-JTE devices as well. Fig. 2 (d) shows a textbook avalanche waveform for USAB-JTE devices under UIS test.

In summary, two single implantation planar edge terminations are demonstrated in this paper, the GR and USAB-JTE. Both the designs are able to achieve positive temperature coefficients, a strong indicator for avalanche breakdown. High efficiencies are also obtained at about 83% for USAB-JTE design and 88% for GR design. Additionally, USAB-JTE shows avalanche robustness under UIS test.