The Packaging Engineer and EMI: Effect of Power Module Architecture on Common Mode Electromagnetic Interference

The leading semiconductor choice for power electronics applications has been silicon (Si) for several decades. Although Si-based power electronics provide the benefit of being mature and well-established, the technology is gradually reaching its limitations. Wide-band gap (WBG) semiconductor devices have started to attract attention due to their higher operating temperatures, faster switching speeds, higher voltage breakdown capability, and lower conduction losses. These device properties of WBG devices result in higher efficiency and power density designs; however, the higher operating frequency, higher operating voltage and faster switching speeds result in an increase in the electromagnetic interference (EMI) footprint of the system. In this work, the common mode (CM) EMI emissions of 12 different module architectures are explored to understand the relationship between the package design and EMI mitigation.

Initially four module architectures are prototyped using 1.2 kV, SiC MOSFET, and their EMI behavior is experimentally evaluated. An LTspice time domain simulation is then built by characterizing the test setup. An in-depth comparative analysis of the EMI spectrums generated by all 12 module architectures is conducted using the time domain simulation developed. CM-equivalent modelling, substitution and superposition principle, and noise transfer functions are then applied to develop insights on how decisions taken with the module architecture can impact the CM emissions of the module. It is found that multilayer architectures can allow high levels of CM current containment; however, for the majority of these multilayer architectures *di/dt* transients become a significant source of CM noise and cannot be ignored. The effect of the addition of decoupling capacitors and filter capacitors into the module architecture is also investigated. It is found that the addition of decoupling capacitors results in an additional resonance peak in the CM EMI frequency spectrum at high frequencies. It is only beyond this resonance peak that EMI mitigation is observed compared to a baseline.

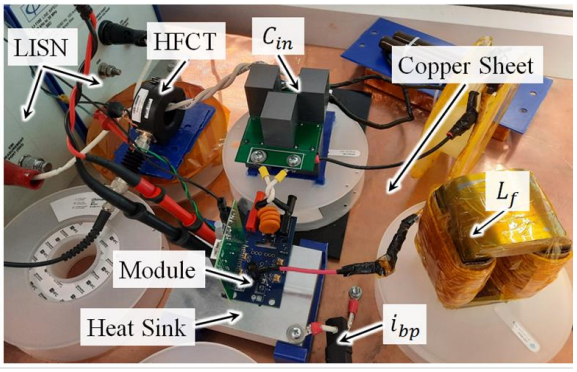

Fig. 1. Hardware setup of EMI testbed

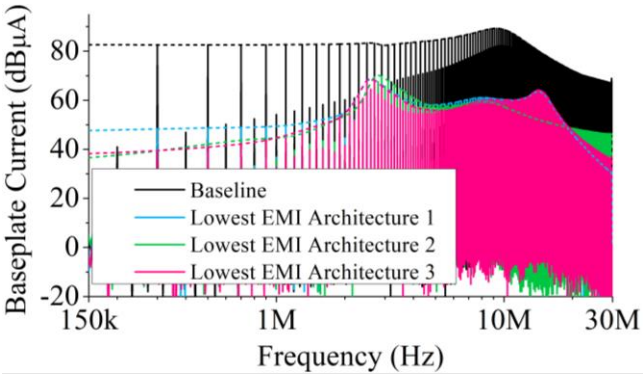

Fig. 2. Simulated EMI spectrum results of the three lowest EMI module architectures compared to a baseline (black)

The three module architectures with the lowest EMI footprint from among the 12 simulated are identified. Although these module architectures are expected to be able to provide noise mitigation up to (and more than) 26 dB compared to a baseline, each architecture requires tradeoffs to be made with either the electrical performance, thermal performance, or manufacturing complexity that must be considered.

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